

Customer No.: 31561
Docket No.: 11555-US-PA
Application No.: 10/605,099

In The Claims

1. (currently amended) An accessing method to a large block [[flash]] memory of a memory device, wherein the large block [[flash]] memory has a plurality of pages and each page has a plurality of sectors~~[[by N]]~~, and the large block memory has two buffers therein to serve as a data cache and a page buffer, wherein the memory device has a controller to control an access operation between a host and the large block memory of the memory device, wherein the controller includes at least two buffers, when the host intends to program the memory device, the method comprising:

transferring data sectors between the host and the large block [[flash]] memory by alternatively using the buffers; [[and]]

issuing a start program command by the controller for programming the large block [[flash]] memory after transferring N-a number of the data sectors with respect to one page;

sending a page of data from the controller to the data cache within the large block memory;

after the data cache is full, shifting a data content in the data cache to the page buffer within the large block memory; and

continuously sending a next page of data to the data cache while a content in the page buffer is programmed to a cell array of the large block memory.

2. (currently amended) The method of claim 1, wherein the at least two buffers in the controller is have-two buffers, and the step of transferring data between the host and the large block [[flash]] memory comprises:

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alternatively using one of the two buffers to store a data transferred from the host;
transferring a previous data stored in the other one of the two buffers to the large block
[[flash]] memory; and
calculating an address for the data to be programmed to the large block [[flash]]
memory by the controller,
wherein at least two of the above three different operations can be performed at the same
time.

3. (cancelled)

4. (currently amended) A method of accessing a large block [[flash]] memory of a
memory device, wherein the large block flash memory has a plurality of pages and each page has
a plurality of sectors~~[[by N]]~~, wherein the memory device has a controller to control an access
operation between a host and the large block [[flash]] memory of the memory device, the
controller also has two buffers regions, the method comprising:

transferring a portion of a current page data from the host to the controller, and
transferring a portion of the current page data from the controller to a data cache within the
large block [[flash]] memory, wherein the two transferring steps can be performed at the same
time;

shifting the current page data in the data cache to the a page buffer within the large block
[[flash]] memory; and

programming the current page data into a cell array of the large block [[flash]] memory,
and simultaneously performing the foregoing two transferring steps if a next page data is desired

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to continuously transfer.

5. (currently amended) The method of claim 4, wherein a "start program with data cache" command is issued to perform ~~in~~ the step of shifting the current page data in the data cache to the page buffer, ~~a command "15H" is issued.~~

6. (original) The method of claim 4, wherein the step of shifting the current page data in the data cache to the page buffer is performed when full data of one page is received and a storage space of the page buffer is available.

7. (original) The method of claim 4, wherein in a time period, at least two of the two transferring steps and the programming step are performed at the same time.

8. (original) The method of claim 4, wherein in a time period, all of the two transferring steps and the programming step are performed at the same time.

9. (currently amended) The method of claim 4, wherein when a last page is received, a "start program10H" command is issued to program the memory cell array

10. (currently amended) The method of claim 4, wherein before a last page is received, a "start program with data cache15H" command is issued for simultaneously receiving the data at the data cache and programming the data at page buffer into the cell array of the large block ~~[[flash]]~~ memory.